REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on December 29, 2000, and the references cited therewith. In this Response, claims 32, 34, 35 and 37 are amended, and new claims 38-39 are added. Accordingly, claims 26-39 are currently pending.

In § 2 of the Office Action, the Examiner stated that it was unclear how the present application could obtain the benefit of an earlier filing date based upon a previous application. Since this Response does not rely upon obtaining an earlier filing date, Applicant does not point out how the present application can obtain such a benefit. However, Applicant reserves the right to establish an earlier effective filing date for one or more of the claims at a later point in time.

Title

In § 4 of the Office Action, the title was objected to as not being descriptive of the invention to which the claims are directed. In response, a new, more descriptive title is provided. While the Office Action states that the title should mention the "'fast page mode', and 'power detection' aspects of the invention", it is respectfully submitted that these aspects of the claims should not be required as part of the title since these aspects are not recited by all of the claims.

§§ 102-103 Rejections of the Claims

In § 6 of the Office Action, claim 37 was rejected under 35 U.S.C. § 102(a) as being anticipated by Tanaka et al. (U.S. Pat. No. 5,325,513). In § 8 of the Office Action, claim 34 was rejected under 35 U.S.C. § 103(a) as being anticipated by Farrer et al. (U.S. Pat. No. 5,307,320) in view of Fung et al. (U.S. Pat. No. 5,630,163). In § 9 of the Office Action, claims 35-36 were rejected under 35 U.S.C. § 103(a) as being anticipated by Tanaka et al. in view of Wyland (U.S. Pat. No. 5,261,064) and Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp. 5-33 thru 5-40, 4/94. In § 10 of the Office Action, claims 26, 29 and 32 were rejected under 35 U.S.C. § 103(a) as being anticipated by Farrer et al. in view of Micron and Wyland. Finally, in § 11 of the Office Action, claims 27-28, 30-31 and 33 were rejected under 35 U.S.C. § 103(a) as being anticipated by Farrer et al., Micron, Wyland and Fung et al.

It is respectfully submitted that each independent claim (i.e., claims 26, 28, 29, 31, 32, 34, 35 and 37), as amended, is allowable over Tanaka et al., Farrer et al., Fung et al., Wyland and Micron, alone or in combination, because none of these references shows or suggests a memory operable in a burst extended data out mode ("burst EDO mode"), as recited by each independent claim. Further, the references do not show or suggest additional elements that are recited by each of the independent claims, as discussed below. Thus, it is respectfully submitted that claims 26, 28, 29, 31, 32, 34, 35 and 37 are allowable. Because claims 27, 30, 33 and 36 depend on claims 26, 29, 32 and 35, respectively, it is respectfully submitted that these claims are also allowable.

As an initial matter, the cited references, alone or in combination, do not show or suggest a memory operable in a "burst EDO mode". As noted in the Summary of the present application, in the burst EDO mode, a "high speed burst of operation is provided where multiple sequential accesses occur following a single column address". Present application, p. 6, lines 5-6. The burst EDO mode has the advantageous characteristics of incrementing the address internal to the memory to eliminate the need for external address lines to switch at high frequencies, and of toggling only one control line (/CAS) per memory chip at the operating frequency in order to clock the internal address counter and the data input/output latches. Present application, p. 6, lines 7-9 and 11-13. The Office Action cites no reference or combination of references that discloses a memory operable in a burst EDO mode. In fact, the Office Action states that Tanaka et al. does not "disclose a first bank of burst access memory coupled to the memory controller", and that "neither Farrer et al. nor Micron discloses a burst mode." Office Action, pp. 6-7, 10. Also, the Office Action does not cite Fung et al. to show a memory with a burst EDO mode.

In an attempt to find a burst EDO memory in the prior art, the Office Action states that "it is well known in the memory art [that] a memory can be operated in a burst mode. For example Wyland discloses burst mode of operation (abstract lines 2-3) in order to increase access time". Office Action, pp. 7, 10. Wyland discloses a dual-port burst access memory (BAM). However, Wyland does not disclose an EDO memory, much less a burst EDO memory. Further, there is no suggestion in any of the references to modify an EDO memory such as that in Micron to operate in burst EDO mode. For example, while Applicant recognized that toggling only one control line (/CAS) per memory chip at the operating frequency during burst EDO mode, thereby eliminating

the need to switch the other control lines and the external address lines, is advantageous because the load on each /CAS control line is typically less than the load on the other control lines and the external address lines because each /CAS typically controls only a byte width of the data bus (present application, p. 6, lines 13-16), the references do not suggest that such a feature would be advantageous. Also, even if it were assumed that the prior art contained a suggestion to modify an EDO memory such as that discussed in Micron to operate in a burst EDO mode (which is not admitted herein), the cited references, alone or in combination, do not contain sufficient technical information to describe a burst EDO memory to a person of ordinary skill in the pertinent art, or to enable such a person to make and to use a burst EDO memory without undue experimentation. Thus, it is respectfully submitted that any suggestion to modify an EDO memory such as that discussed in Micron to operate in a burst EDO mode, or any teaching of how to make and use a burst EDO memory, could only have been derived at by the Examiner through the impermissible use of hindsight based on the disclosure of the present application. As stated in MPEP §2143.01, an assertion that the claimed invention may be within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish *prima facie* obviousness. Thus, it is respectfully submitted that each of independent claims 26, 28, 29, 31, 32, 34, 35 and 37 is allowable at least because the cited references do not show or suggest a memory operable in a burst EDO mode.

In addition, it is respectfully submitted that claims 26, 28, 29 and 31 are also allowable because the cited references do not show or suggest a memory which has "a first set of access control signal timing requirements for the burst EDO mode", that claims 32 and 34 are also allowable because the cited references do not show or suggest a memory which has "a first set of access control signals for operation in the burst EDO mode", and that claims 35 and 37 are also allowable because the cited references do not show or suggest access control signals for providing access to a bank of burst EDO memory. In particular, since the cited references do not show or suggest a burst EDO memory, it therefore follows that the cited references also do not show or suggest access control signals that could be used for accessing a burst EDO memory.

In addition, it is respectfully submitted that claims 26, 28, 29, 31, 32, 34, 35 and 37 are also allowable because the cited references do not show or suggest a memory controller that can provide a first set of access control signals for accessing a burst EDO memory and a second set

of access control signals for accessing a memory of a second operation mode. In particular, since the cited references do not show or suggest access control signals that could be used for accessing a burst EDO memory, it therefore follows that the cited references also do not show or suggest a memory controller that can provide such first and second sets of access control signals.

New Claims

New claims 38-39 are also believed to be allowable over the cited references.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration and allowance of the application. Please charge any additional fees deemed necessary, or credit any overpayment, to Deposit Account 19-0743. The Examiner is invited to telephone Applicant's attorney at 612-373-6975 to facilitate the prosecution of this application.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 2nd day of February, 2001.

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